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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/766,746

01/27/2004

Tie Wang

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22898

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09/02/2005

THE LAW OFFICES OF MIKIO ISHIMARU  
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EXAMINER

DOLAN, JENNIFER M

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/766,746

**Applicant(s)**

WANG ET AL.

**Examiner**

Jennifer M. Dolan

**Art Unit**

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 1/27/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,933,176 to Kirloskar et al.

Regarding claims 1, 6, 11, 15, 16, and 20, Kirloskar discloses a method for fabricating a semiconductor package, comprising: providing a substrate (122) in a continuous strip format (figures 3a-3b; column 4, lines 15-17); attaching semiconductor devices (124) in a continuous strip format to the substrate (figure 3b; column 4, lines 18-26); applying an underfill between the semiconductor devices and the substrate (column 4, lines 26-30); applying a thermal interface material (136) to the upper faces of the semiconductor devices opposite the substrate (figures 3F, 7F; column 4, lines 38-42; column 6, lines 10-24); attaching a flat panel heat spreader (132) to each semiconductor device by means of the thermal interface material (figures 3I, 5I, 7H); curing the thermal interface material (column 6, lines 10-24); encapsulating the semiconductor devices and portions of the flat panel heat spreader (column 4, line 60 – column 5, line 3) with open encapsulation, leaving the surface of the heat spreader opposite the substrate externally exposed (figures 3I, 5I); attaching ball grid arrays (130) to the substrate opposite the semiconductor

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devices (see figures 3I, 3J; column 5, lines 4-15); and singulating individual semiconductor packages from the strip format (column 5, lines 15-19; figure 3I-3J).

Regarding claims 2, 7, 12, and 17, Kirloskar discloses that the flat panel heat spreader may be applied in a pre-cut flat panel configuration (column 6, lines 1-15; figure 7G).

Regarding claims 3, 4, 8, 9, 13, 14, 18, and 19, Kirloskar discloses that the heat spreader is a continuous flat panel heat spreader attached over substantially the entire strip format (figures 3D, 3I; column 4, lines 30-37), and that the heat spreader is cut into individual panels following the attachment of the heat spreader (figures 3I-3J; heat spreader is cut into individual panels during the singulation step, which occurs after attaching the heat spreader).

Regarding claims 5 and 10, Kirloskar discloses that the heat spreader is attached by the encapsulant, and hence, must necessarily be physically attached after the encapsulant is dispensed (see Kirloskar, column 4, line 60 – column 5, line 3).

3. Claims 1-4 and 11-15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,734,552 to Combs et al.

Regarding claims 1, 11, and 15 Combs discloses a method for fabricating a semiconductor package, comprising: providing a substrate (100) in a strip format (column 3, lines 50-55), attaching semiconductor devices (130) in a strip format to the substrate (column 4, lines 20-25); applying a thermal interface material (119, 120) to the semiconductor devices (column 5, lines 35-45; column 6, lines 1-15); attaching a flat panel heat spreader (110, 112) to each semiconductor device (column 5, lines 1-20); encapsulating the semiconductor devices with open encapsulation, leaving the surface of the heat spreader opposite the substrate externally

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exposed (figure 1; column 5, lines 20-35; column 6, lines 15-25); and singulating individual packages from the strip format (column 6, lines 28-37).

Regarding claims 2 and 12, Combs discloses that the heat spreaders can be pre-cut (column 5, lines 1-6).

Regarding claims 3, 4, 13, and 14, Combs discloses that the heat spreaders can be provided in a continuous flat panel (figures 9a, 9b; column 5, lines 1-20) and cut into individual heat spreader panels (upon singulation).

### *Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 6,309,915 to Distefano discloses using a continuous strip heat spreader for a strip-format packaging operation.
- b. U.S. Patent No. 6,853,070 to Khan et al. discloses the use of open encapsulation for discrete heat spreaders.
- c. U.S. Patent Publication No. 2002/0149092 to Lee discloses a strip package assembly using a heat spreading lid portion.
- d. U.S. Patent No. 6,559,537 to Bolken et al. discloses chip packaging using a strip-format substrate and a strip-format heat spreader.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan  
Examiner  
Art Unit 2813

jmd

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
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